ABSTRACT OF THE DISCLOSURE

[0063] Viterbi decoding is implemented using an asymmetrical trellis 70 having an A-trellis 72 and a B-trellis 74. The trellis 70 is designed for efficient implementation on a processing device 40 with arithmetic units 42 having multi-field arithmetic and logic capabilities By concurrently processing multiple path metrics in separate fields, a highly efficient decoder may be implemented in a software-controlled device.